

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Ravi Iyer

Serial No.: 09/059,865

Filed: April 14, 1998

For: PLANARIZATION USING PLASMA
OXIDIZED AMORPHOUS SILICON



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Group Art Unit: 2813

Examiner: Nguyen, T.

Atty Docket: MICS:0015--2/FLE
93-118.02

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

CERTIFICATE OF MAILING 37 C.F.R. 1.8	
I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:	
January 7, 2000	<i>Kim Hennessey</i>
Date	Kim Hennessey

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 1.191 AND 1.192

This Appeal Brief is being filed in triplicate along with the Notice of Appeal mailed herewith on January 7, 2000.

1. **REAL PARTY IN INTEREST**

The real party in interest is Micron Technology, Inc., the Assignee of the above-referenced application by virtue of the Assignment recorded at reel 8190, frame 0268, and dated February 12, 1996.

2. **RELATED APPEALS AND INTERFERENCES**

Appellant is unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellant's legal representative in this Appeal. Micron Technology, Inc., the

Assignee of the above-referenced application, as evidenced by the documents mentioned above, will be directly affected by the Board's decision in the pending appeal.

3. STATUS OF CLAIMS

Claims 12-23 have twice been rejected and, thus, are the subject of this appeal.

4. STATUS OF AMENDMENTS

No final rejection has been issued, and there are no outstanding amendments that have not been entered.

5. SUMMARY OF THE INVENTION AND OF THE DISCLOSED EMBODIMENTS

Referring to Fig. 6, many semiconductor processes involve the deposition of a blanket layer 602, such as silicon, over protruding device features 601. Page 13, lines 20-22. As illustrated in Fig. 7, the layer 602 is patterned and etched to clear areas where the layer 602 is not needed -- to expose source or drain regions on either side of a gate electrode, for instance. Page 13, lines 22-29. This removal process often leaves undesirable residue, typically referred to as "stringers," that is difficult to remove without damaging the adjacent structures. Page 13, line 29, to page 14, line 2. However, if this material is non-dielectric in nature, it may cause gate leakage. Page 14, lines 16-19. Therefore, rather than risk damaging the adjacent structures by attempting to remove these stringers, Appellant instead oxidizes or nitridizes the undesirable non-dielectric stringers to form innocuous dielectric material that need not be removed. Page 14, lines 3-21; Fig. 8.

6. **ISSUES**

Issue No. 1:

Whether claims 18-23 are unpatentable under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, has possession of the claimed invention.

Issue No. 2:

Whether claims 12-23 are unpatentable under 35 U.S.C. 103(a) as being obvious over the Kim '637 reference in view of the Matsuoka '508 reference.

Issue No. 3:

Whether claims 12-23 are unpatentable under the judicially created doctrine of obviousness-type double patenting over claims 1-22 of U.S. Patent No. 5,872,052.

7. **GROUPING OF CLAIMS**

Independent claims 12 and 18 will stand or fall separately. Dependent claims 13-17 will stand or fall with independent claim 12. Dependent claims 19-23 will stand or fall with independent claim 18.

8. **ARGUMENT**

As discussed in detail below, Appellant respectfully submits that the Examiner has misinterpreted clear claim language and misapplied long standing principles of law in

formulating and maintaining the outstanding rejections. Thus, Appellant respectfully requests that the Board favorably consider the remarks set forth below, withdraw the outstanding rejections, and allow claims 12-23.

Issue No. 1

In the present Official Action (Paper No. 12), the Examiner rejected claims 18-23 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification. Specifically, the Examiner stated:

The limitation “undesirable residual” in claim 18 contains subject matter which was not described in the original specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor. It is suggested to delete “undesirable”.

Appellant respectfully traverses the Examiner’s rejection. To maintain a rejection under 35 U.S.C. 112, the Examiner has the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize from the disclosure a description of the invention defined by the claims. *In re Wertheim*, 191 U.S.P.Q. 90, 98 (C.C.P.A. 1976). Section 2163 of the Manual of Patent Examining Procedure, which is supposed to guide Examiners during the examination of a patent examination, clearly sets forth the standard for determining compliance with the written description requirement of 35 U.S.C. 112, first paragraph. Specifically, M.P.E.P. § 2163.02 states:

[T]he fundamental factual inquiry is whether a claim defines an invention that is clearly conveyed to those skilled in the art at the time the application was filed. The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement.

In a previous Response to an Official Action (Paper No. 6), Appellant amended claims 18, 22 and 23 by adding the descriptive term “undesirable” to modify to the claimed element, “residual non-dielectric material,” which is recited as being left in some of the creases between protruding features on a substrate after a portion of the non-dielectric material is removed. It is beyond question that the *residual* non-dielectric material which is left in the creases is inherently “*undesirable*.” Indeed, the undesirability of the residual material is clearly described in the specification. In particular, the specification sets forth:

Many semiconductor processes involve forming a blanket deposited layer 602 over protruding device features 601. In particular, polysilicon or amorphous silicon are commonly used to form capacitor structures or device contacts. As shown in FIG. 7, layer 602 is patterned and etched to clear areas where layer 602 is not needed. This is done, for example, to expose source and drain regions on either side of a gate electrode. *The removal process, however, often leave “stringers” 701 as a residue that are difficult to remove without damaging the structure or topology of protruding features 601. . . . In the specific example of a gate electrode with polysilicon stringers, the stringer 701 causes gate leakage*

Specification, pages 13-14 (emphasis added).

Admittedly, the descriptive term “undesirable” is not used in conjunction with the term “residue.” However, it is simply inconceivable to imagine how one skilled in the art could fail to appreciate, based both on experience and from the above description, that such residue could be anything but inherently “undesirable.” If such residue left in creases were not “undesirable,” there would be no reason for discussing the difficulty in removing the residue and presenting innovative methods for neutralizing such residue. Moreover, it is difficult to understand how one skilled in the art could possibly believe that residue that detrimentally

affects component performance, such as residue (i.e., polysilicon stringers) left about a gate electrode which causes gate leakage, could be anything but “undesirable.”

In further support of the inherency of the undesirability of the claimed residue, Appellant directs the Board’s attention to the Examiner’s own statement set forth in the Official Action mailed January 25, 1999 (Paper No. 7). In response to Appellant’s argument, the Examiner asserted that:

Applicant contends that none of the reference teaches the stringers (spacers 18) are undesirable features. In response to applicant, it is asserted that the conductive stringers (spacers, 18) are *known to be undesirable features* that causes shorts with conductor

Paper No. 7, page 4 (emphasis added). Clearly, even the Examiner believes that it is well-known that residue left in creases, such as the residue or “stringers” described in the specification, are inherently “undesirable.”

Further, should an attempt be made to reject claims 18-23 as containing new matter, such a rejection would not be well-founded. M.P.E.P. § 2163.07(a) states:

By disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter.

The standards set forth in the M.P.E.P. have been applied by both the C.C.P.A. and the Federal Circuit in determining whether the addition of descriptive matter to the

specification and to the claims should be prohibited as constituting “new matter.” For example, in *In re Nathan*, 140 U.S.P.Q. 601 (C.C.P.A. 1964), the C.C.P.A. reversed a new matter rejection, holding that a later-added limitation to the claims was “an inherent characteristic” of the claimed subject matter. The court explained that “a subsequent clarification of or a change in an original disclosure does not necessarily make that original disclosure fatally defective.” *Id.* at 603.

— In *Kennecott Corp. v. Kyocera Int’l Inc.*, 5 U.S.P.Q.2d 1194 (Fed. Cir. 1987), the Federal Circuit followed the reasoning set forth in *In re Nathan*. In *Kennecott*, the Federal Circuit held that the claims of a patent were entitled to the benefit of the earlier filing date of a parent application despite the addition of descriptive matter in the specification and claims of the later-filed application. In determining that the additional matter did not constitute “new matter,” the Federal Circuit explained:

The disclosure in a subsequent patent application of an inherent property of a product does not deprive that product of the benefit of the earlier filing date. Nor does the inclusion of a description of that property in later-filed claims change this reasonable result.

Kennecott, 5 U.S.P.Q.2d at 1198.

As discussed above, the undesirability of the claimed residue is disclosed in the specification and, in any event, those skilled in the art would recognize the undesirability of such residue. Further, it can be gleaned from the above-stated standards that it is improper for the Examiner to reject a claim as reciting new matter simply because the identical, added descriptive term cannot be found verbatim in the specification. Moreover, it is improper for the Examiner to

reject such a claim if the added term is merely a description of a property or characteristic that is inherent in the claimed element.

In view of the above, it is respectfully submitted that the Examiner has failed to satisfy the Examiner's requisite burden of establishing a *prima facie* case that the addition of the descriptive term "undesirable" violates the requirements of Section 112 or constitutes new matter. Further, it is believed that the Examiner's rejection is improper because "undesirable" is nothing more than an inherent characteristic of the claimed and described residue. Such undesirability is clearly described in the written description of the invention. Accordingly, withdrawal of the rejection under 35 U.S.C. 112, first paragraph, is respectfully requested.

Issue No. 2

In the present rejection, the Examiner relied on a misplaced interpretation of certain claim terms that were explained more fully in the first rejection. Therefore, before discussing the present rejection, Appellant believes that it may be helpful for the Board to consider the first rejection and Appellant's response.

In the First Official Action, the Examiner rejected claims 12-16 and 18-22 under 35 U.S.C. § 102(e) as being anticipated by the Kim patent. Specifically, the Examiner asserted that the silicon spacers disclosed in the Kim patent are "the same as applicant's non-dielectric stringers."

In response, Appellant noted that “spacers” and “stringers” are terms of art that denote two different structures. As known to those skilled in the art, and as discussed in detail in the above-referenced application, e.g., pages 13 and 14, “stringers” are small, undesirable residuals that are typically left in creases on a substrate after an etching process. “Spacers,” on the other hand, are desirable features that are specifically designed and fabricated for various purposes by those of ordinary skill in the art. In short, in the context of the rejected claims, these two terms are *not* the same, equivalent, or interchangeable.

As specifically noted in regard to independent claim 12, none of the references of record disclose or suggest the removal of a portion of a layer of non-dielectric material, leaving stringers of the dielectric material in the creases on the integrated circuit, and converting these stringers of non-dielectric material into a dielectric material. As stated in the application beginning on page 13, line 29, the complete removal of these residual stringers is difficult without damaging the structure or topology of protruding features of the integrated circuit. However, in the prior art, a lose-lose situation existed because residual non-dielectric stringers, such as polysilicon stringers, may cause undesirable gate leakage. *See* page 14, lines 16-21. The subject matter set forth in claim 12 solves this problem by converting the stringers of non-dielectric material into a dielectric material. Because none of the prior art of record, either alone or in combination, discloses or suggests the method set forth in independent claim 12, Appellant argued that claims 12-17 were patentable over the prior art of record.

As further noted in regard to independent claim 18, none of the references of record, either alone or in combination, disclose or suggest the attempted removal of non-dielectric

material from creases where the removal method leaves undesirable residual non-dielectric material in some of the creases, along with the conversion of the undesirable residual non-dielectric material into a dielectric material. Appellant amended claims 18, 22, and 23 to clarify that this residual non-dielectric material is undesirable, unlike the desirable spacers disclosed in the Kim patent that are specifically designed and engineered to form a particular structure which performs a specific purpose. As discussed above in regard to claim 12, Appellant has solved the problem by converting the undesirable non-dielectric material that may adversely affect the ultimate functioning of the circuit into an innocuous dielectric material. Since none of the prior art of record discloses the problem, much less the solution to the problem as set forth in independent claim 18, Appellant argued that claims 18-23 were patentable over the prior art of record.

The Board should be aware that the Examiner withdrew the rejection under Section 102 in view of these arguments. However, the Examiner maintained a rejection under Section 103 in both the Second Official Action (Paper No. 7), which has been withdrawn by the Examiner, and in the present Official Action (Paper No. 12). Specifically, in the present Official Action (Paper No. 12) which is the subject of this appeal, the Examiner rejected claims 12-23 under 35 U.S.C. § 103(a) as being obvious over the Kim patent in view of the Matusoka patent. Specifically, the Examiner stated:

Kim teaches a method of manufacturing an integrated circuit comprising the steps of: forming features on a substrate, the features protruding from the substrate to create creases adjacent the features (12, 13, 14), depositing a layer of non-dielectric material (stringer) (18, silicon) over the features and the creases, removing a portion of the non-dielectric material from the creases using a given method, leaving undesirable residual non-dielectric material in some of the creases, and converting the undesirable residual

non-dielectric material in the creases into a dielectric material (22, oxide) (see figures 1-2, col. 2, lines 50-68).

However, the reference does not teach removing a portion of the non-dielectric material, and nitridizing the non-dielectric material.

It is well-known in the art to form a non-dielectric material (silicon) over the protruding on substrate.

Therefore, it would have been obvious to one of ordinary skill in the requisite art at the time of the invention was made to remove a portion of the non-dielectric material to left the undesirable residual because the technique is well-known in the art.

Matsuoka et al teaches that silicon nitride side walls may be used, rather than silicon oxide (see column 16, lines 10-15).

Therefore, it would have been obvious to one of ordinary skill in the requisite art at the time of the invention was made to provide silicon nitride sidewall, in place of oxide sidewalls, in the Kim process, as taught by Matsuoka et al because it is shown that it is known in the art that silicon nitride function effectively as a sidewall and because silicon nitride is a better diffusion barrier and etch stop than silicon oxide and would therefore better protect the gate electrode.

In response to Appellant's previous arguments, the Examiner further stated:

Applicant contends that none of the reference teaches the stringers (spacers 18) are the undesirable residual. In response to applicant, the limitation "undesirable residual" contains subject matter which was not described in the original specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor. The non dielectric residual remaining after etching step is conductive stringers (spacers, 18). Therefore it would have been obvious to the artisan to form oxide by oxidizing the stringers (spacers, 18).

Appellant respectfully traverses this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214

U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the

teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

As can be seen from this rejection, the Examiner has merely relied on the Matusoka patent to teach that silicon nitride sidewalls may be used instead of the silicon oxide sidewalls disclosed in the Kim patent. The Examiner has maintained reliance on the Kim patent for the remainder of the claimed subject matter and has continued improperly to equate the “spacers” of the Kim patent with the “stringers” and “undesirable residual non-dielectric material” set forth in independent claims 12 and 18, respectively.

However, as discussed above, the Kim patent is not directed to the treatment of undesirable residue as set forth in the rejected claims. Rather, the Kim patent clearly discloses a method that *uses a spacer* for forming a self-aligned contact. Kim, col. 1, lines 9-12. During the

formation of the contact, “*silicon spacer 18 ... is formed by common spacer-forming methods* at the side wall of the gate electrode 13 and upper surface of the interlayer oxide 14.” Kim, col. 2, lines 51-54; Fig. 1B (emphasis added). Thereafter, a mask 20 is formed and various layers are etched subsequent to filling the contact hole 10 with metal wiring 21. Kim, col. 3, lines 1-23; Figs. 1C and 1D. The Kim patent describes the advantages of “reducing the contact area due to the increase of contact mask tolerance for making the contact hole by forming a silicon spacer ... [and] thermally oxidizing the part or the whole of the above-said silicon spacer.” Kim, col. 4, lines 1-8. Thus, the Kim patent unquestionably discloses that a “spacer” is a desirable feature that is purposefully manufactured and used to produce a contact having certain advantages over conventional contacts.

As can be seen, the actual disclosure of the Kim patent illuminates the speciousness of the Examiner’s attempts to equate Kim’s silicon spacers 18 with the claimed “stringers” and “undesirable non-dielectric material.” Clearly, Kim’s silicon spacers 18 are neither. Thus, Appellant respectfully asks the Board to note that the Examiner’s interpretation of the Kim reference is inaccurate and nothing more than a blatant and improper usage of hindsight.

Like the Kim patent, the Matusoka patent is also not related to problems arising from undesirable non-dielectric residuals remaining after an etching step. Therefore, the addition of the Matusoka patent to the present combination does not cure the deficiencies of the Kim patent highlighted above. Accordingly, even if the Examiner can combine these references, the combination still fails to disclose or suggest that a nitridizing or an oxidizing method may be used to convert undesirable non-dielectric residue, such as stringers, into innocuous dielectric

material as claimed. Indeed, the Board should note that those skilled in the art attempt to *prevent* formation of these undesirable residuals through improved etching techniques, rather than rendering the undesirable residuals harmless after formation as disclosed and claimed by Applicant.

In view of the remarks set forth above, Appellant respectfully submits that the Examiner has failed to demonstrate a *prima facie* case of obviousness as required. Specifically, the Examiner has misinterpreted the Kim patent and the pending claims, apparently due to an improper use of hindsight. Therefore, Appellant respectfully requests that the Board withdraw the outstanding rejection and allow claims 12-23.

Issue No. 3:

The Examiner has also rejected claims 12-23 based on the judicially created doctrine of obviousness-type double patenting in view of U.S. Patent No. 5,872,052. Specifically, the Examiner stated:

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: a method of manufacturing an integrated circuit, depositing a layer of non-dielectric material (silicon) over the substrate and remove the substrate leaving the residual non-dielectric material, converting the non-dielectric residual material into dielectric material.

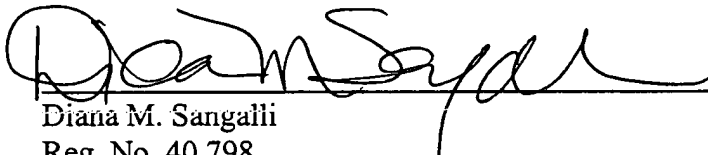
Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Although Appellant disagrees with this rejection, Appellant recognizes that filing a Terminal Disclaimer to obviate this rejection will facilitate the prompt issuance of a patent without any real loss of patent term or other rights for the assignee. Specifically, it is noted that the present application is a continuation of application Serial No. 08/599,675, filed on February 12, 1996, which issued as the '052 patent. Thus, under 35 U.S.C. § 154, the term of both the '052 patent and any patent issuing from the present application is set to expire twenty years from the date of the earliest original filing, i.e., February 12, 1996, regardless of whether a Terminal Disclaimer is filed. Although the Terminal Disclaimer further requires that the assignee maintain common ownership of these three patents, the assignee has no intention of dividing ownership in any event. Therefore, should the Board withdraw the outstanding rejection and allow claims 12-23 as respectfully urged herein, Appellant will file an appropriate Terminal Disclaimer to obviate this remaining rejection.

As explained in the Transmittal Letter accompanying this Appeal Brief, the requisite fee for filing an Appeal Brief was paid when the previous Appeal Brief was mailed on September 7, 1999. However, the Commissioner is authorized to charge any additional fees which may be required, to Deposit Account No. 13-3092; Order No. MICS:0015--2/FLE (93-118.02).

Respectfully submitted,

Date: -January 7, 2000



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9. **APPENDIX OF CLAIMS ON APPEAL**

12. A method of manufacturing an integrated circuit, the method comprising the steps of:

- (a) forming features on a substrate, the features protruding from the substrate to create creases adjacent the features;
- (b) depositing a layer of non-dielectric material over the features and the creases;
- (c) removing a portion of the layer of non-dielectric material, leaving stringers of the non-dielectric material in the creases; and
- (d) converting the stringers of non-dielectric material in the creases into a dielectric material.

13. The method, as set forth in claim 12, wherein step (a) comprises the step of forming gate electrodes protruding from the substrate.

14. The method, as set forth in claim 12, wherein step (b) comprises the step of depositing a layer of silicon over the features and the creases.

15. The method, as set forth in claim 12, wherein step (c) comprises the step of etching the portion of the layer of non-dielectric material.

16. The method, as set forth in claim 12, wherein step (d) comprises the step of oxidizing the stringers.

17. The method, as set forth in claim 12, wherein step (d) comprises the step of nitridizing the stringers.

18. A method of manufacturing an integrated circuit, the method comprising the steps of:

- (a) forming features on a substrate, the features protruding from the substrate to create creases adjacent the features;
- (b) depositing a layer of non-dielectric material over the features and the creases;
- (c) removing a portion of the non-dielectric material from the creases using a given method, the given method leaving undesirable residual non-dielectric material in some of the creases; and

- (d) converting the undesirable residual non-dielectric material in the creases into a dielectric material.

19. The method, as set forth in claim 18, wherein step (a) comprises the step of forming gate electrodes protruding from the substrate.

20. The method, as set forth in claim 18, wherein step (b) comprises the step of depositing a layer of silicon over the features and the creases.

21. The method, as set forth in claim 18, wherein the given method comprises an etching method.

22. The method, as set forth in claim 18, wherein step (d) comprises the step of oxidizing the undesirable residual non-dielectric material.

23. The method, as set forth in claim 18, wherein step (d) comprises the step of nitridizing the undesirable residual non-dielectric material.